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10/589,428	05/02/2007	**Kengo Maeda**	559502005400	9457

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EXAMINER	
RADKE, JAY W	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/589,428	MAEDA ET AL.	
	Examiner	Art Unit	
	JAY RADKE	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 May 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/10/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description:

The references "COAPLUS", "COAMINUS", "FINEPLUS", "FINEMINUS" and "EXTRAMINUS" are not in FIG. 2.

2. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

1. The abstract of the disclosure is objected to because minor informalities/translation/grammar problems. Examiner suggests writing the abstract to read as follows, wherein added language or punctuation has been underlined or bracketed while removed language has been double strikedout for emphasis:

A semiconductor memory[,] using a DLL circuit having a phase comparison circuit for comparing the phase ~~phases~~ of an internal clock to that of ~~and~~ a delay clock and a variable delay addition circuit for adjusting delay amount according to a signal from the phase comparison circuit[,] comprises a means for inputting a first signal[,] latched as ~~to~~ a logic "1" by start of one clock cycle of the internal clock[,] to the variable delay addition circuit through a dummy delay at the start of burst and a means for detecting the duration time of the logic "1" of the first signal inputted by the variable delay addition circuit through the dummy delay until one clock cycle of the internal clock is completed and setting the initial value of delay amount of the variable delay addition circuit based on the duration time.

Correction is required. See MPEP § 608.01(b).

2. The **title** of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "**SEMICONDUCTOR MEMORY USING A DLL CIRCUIT**".

3. The disclosure is objected to because of the following informalities:

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. The application is often awkward to read at best substantially due to translation problems. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification especially after paragraph [0066].

Examiner will address below problems with the specification up to paragraph [0066].

Regarding [0006]: The reference "Δt" does not match "Dt" in FIG. 18. Please make them match. Examiner suggests changing "Dt" to "Δt" in FIG. 18 since there are several instances of "Δt" in the specification.

Regarding [0010]: Examiner suggests changing "uselessly" to "unnecessarily" or "needlessly".

Regarding [0012, 0013, 0014, and 0017]: "DDL" is a typographical error and should be corrected to read as "DLL".

Regarding [0031] (line2 of page 14): "resister" is a typographical error and should be corrected to read as "register".

Regarding [0040]: “detects an falling edge” should be corrected to read “detects a falling edge”.

Regarding [0042] (lines 1-3 of page 17): The logical priority or meaning is not clear in the phrase "When the clock control circuit 2 detects a falling edge of the chip enable signal CE# or the address effective signal ADV# and both the signals become effective, the clock control circuit 2 outputs the burst start signal ST".
Is ST outputted when both CE# and ADV# become effective and either a falling edge of CE# is detected or the falling edge of ADV# signal is detected?
Is ST outputted when both CE# and ADV# become effective and either a falling edge of CE# is detected or ADV# signal is detected?
Could it be that ST is outputted when ADV# is detected when both ADV# and CE# are effective or when a falling edge of CE# is detected?
What does "effective" mean exactly? If effective means active low then a logical OR already includes the case of both signals being effective so "and both signals become effective" is redundant and adds confusion to the sentence.

Perhaps rewriting the sentence as “When the clock control circuit 2 detects a falling edge of the chip enable signal CE# or the address effective signal ADV# or when both

the signals become effective low, the clock control circuit 2 outputs the burst start signal ST" will fix the problem.

Regarding [0047]: The references "COAPLUS", "COAMINUS", "FINEPLUS", "FINEMINUS" and "EXTRAMINUS" are not in FIG. 2.

Regarding [0051]: Examiner can not make sense of "The clock control circuit 2 in Fig. 1 detects the falling edge of the chip enable signal CE# or the address effective signal ADV# and the burst start signal ST output when both the signals become effective is input to the control circuit 100 of the DLL circuit 6". There are so many ways to interpret or misinterpret the logical meaning of this sentence along with guesses to the proper grammar and punctuation that was intended by Applicant. There are too many scenarios to go into detail. Please correct.

Examiner suggest inserting "rather is" into line 1 of page 21 so that the sentence reads as "However, the operation clock CF is not a clock having periodicity but rather is a signal of "H" level being output at the falling edge of the internal clock C2 from an RS flip flop".

Regarding [0055]: Is difficult to understand giving the awkward and vague use of the phrase "counterpart thereof" three times and a reference to an operation "A105" that is ether being defined or is meant to refer to a drawing but Examiner can not find a drawing with this reference. Perhaps using the word "corresponding" would be better

than "counterpart of" or "counterpart thereof". Examiner suggests rewriting the paragraph as:

"At the time when the clocked inverter becomes disabled by the "H" level of the write signal WT, the coarse register 402 of each stage of the coarse delay circuit 400 determines the stage that the operation clock C4 has reached according to the logic level ("H" or "L" level) of the corresponding coarse delay cell 401. Then the write signal WT becomes "L" level and the coarse register 402 of each stage writes the determination result. However, at the time when the clocked inverter is disabled and the operation clock C4 is stopped, "H" is written to only the coarse register 402 that corresponds to the coarse delay cell 401 that in turn corresponds to the stage that the operation clock C4 has reached."

Regarding [0056]: "the DQ buffer" is referred to in the specification several times; however, there is no DQ buffer found in the figures. A DQ buffer delay was labeled in the FIG. 18 that illustrates a timing diagram of the Prior Art; however, a DQ buffer has not been illustrated to be present in any of the figures of the invention. If "DOUT Buffer 14" of FIG. 1 is meant to be "the DQ buffer" then box 14 of FIG. 1 should be updated to perhaps be labeled as "DOUT or DQ buffer".

The grammar and punctuation makes this paragraph difficult to read and/or understand. Examiner suggests changing the sentence beginning with "In the case where" to "In the case where delay at the DQ buffer becomes large due to poor performance of the DQ buffer or due to a high used frequency (internal clock delay or

DQ buffer delay is increased that is) causes the external clock and the DQ output to be unable to be synchronized (setup time can not be ensured) by just canceling the internal clock delay, delay of the DQ buffer can then be cancelled by configuring the circuit to determine whether or not the relationship "dummy delay by the dummy delay circuit 200 + coarse delay by the coarse delay circuit 400 + dummy delay corresponding to DQ buffer delay = external clock of 2 cycles" is met."

Regarding [0061]: The first sentence of this paragraph is inconsistent with FIG. 3. Perhaps this sentence should read as "During operation in this lock mode (initial clock output), the DLL clock C3 can be generated to be in sync with the rising edge of the external clock C1 starting at the fifth clock of the external clock C1." The clock C3 is not illustrated in FIG. 3 to be in sync with C2 (follow the vertical dashed line).

Regarding [0063]: Examiner suggests changing "a logical AND (AND) between" to "a logical AND of".

Regarding [0064]: Examiner suggests changing "determines the phase" to "determines if the phase".

Regarding [0065, 0066]: Again, FIG.2 does not have reference labels "COAPLUS", "COAMINUS", "FINEPLUS", "FINEMINUS" and "EXTRAMINUS".

Appropriate correction is required.

Claim Objections

3. Claim 6 is objected to because of the following informalities:

Regarding claim 6: A device comprising "a function" does not make sense. There needs to be structure claimed since this is a device claim.

For the purpose of examination, Examiner will interpret the last paragraph of claim 6 to read as follows:

a switching means to switch the DLL circuit between use and nonuse by user setting with a command decoder for decoding an address signal for specifying a user-specified command and a data signal for specifying a user-specified command, and a command register for storing the output of the command decoder as the lock mode after the initial setting of the delay amount in the variable delay addition circuit.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 2, and 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 1, 2, and 3:

A delay between a delay and an external clock does not make sense especially since the specification teaches there being a delay between two clocks, an internal clock and an external clock, such as in [0006].

Considering this, then it seems correcting claims 1,2, and 3 would involve changing “an internal clock delay” to “an internal clock”; however with or without this correction there is an antecedent basis problem, wherein “a means for inputting a first signal outputted during one clock cycle of the internal clock” would be indefinite since there would be two prior references of "an internal clock" and it is not clear to which one is being referred. Furthermore, the specification teaches that the first internal clock or delay of an internal clock is indeed not referring to the same internal clock that is being inputted into the phase comparator (see FIG. 2, the internal clock that has a delay from the external clock having the value dummy delay is Delay Clock C6 and the internal clock that is being compared to the Delay Clock is Reference Clock C5); hence the specification teaches “an internal clock delay” on line 2 of the claim and "an internal" clock on line 5 of the claim refer to two different internal clocks so it is indefinite as to which internal clock "the internal clock" on line 10 of claim 1 is referring. Even further problems, the specification teaches the "delay clock" being the internal clock that is

delayed by Dummy Delay from the external clock ([0009, 0064]; Delay Clock C6 is delayed by Dummy Delay; also see FIG. 2) so therefore the specification teaches the first instance of "an internal clock" on line 2 of claim 1 is the very same delay clock that is referred to on line 6 of claim 1. Considering all or any of the above, this claim is indefinite.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-3, 5, 6, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Matsuzaki et al. (US 6,088,255; hereinafter "Matsuzaki").

Regarding claim 1: In so far as definite Matsuzaki teaches a semiconductor memory using a DDL circuit (FIG. 5) having a dummy delay (DUMMY-DATA-OUTPUT BUFFER and DUMMY-INPUT BUFFER) corresponding to delay between an internal clock (the clock signal outputted from 1028) delay and an external clock (CLK), a variable delay addition circuit (the clock-cycle measurement unit without basic dleay1025, DELAY-CONTROL CIRCUIT 1040, 1022) having a means for adjusting delay amount by a delay amount adjusting signal (the signal outputted from DELAY-CONTROL CIRCUIT 1040), and a phase comparison circuit (PHASE COMPARISON CIRCUIT 1030) for

comparing a phase of an internal clock (CLK2) with that of a delay clock (the internal clock outputted from 1028) inputted through the variable delay addition circuit and the dummy delay and outputting the delay amount adjusting signal (output from DELAY-CONTROL circuit 1040) to the variable delay addition circuit (input to 1022), the semiconductor memory comprising:

a means for inputting a first signal outputted during one clock cycle of the internal clock to the variable delay addition circuit through the dummy delay at a start of burst (the DLL control circuit 1060 suspends the supply of CLK2 to the phase-comparison circuit, DLL, during a predetermined time period after a start of power supply to the semiconductor device or switching of operation mode from stand-by to a normal operation mode, burst mode is interpreted to be a normal operation mode such as read or write, and then the clock-cycle measurement unit 1050 measures a delay during one clock cycle of the clock CLK1 and outputs an obtained result to the delay-control circuit 1040; column 4, lines 5-12; column 23, lines 38-67) ; and

a means for detecting duration time of an active logical value of the first signal inputted from the variable delay addition circuit through the dummy delay until one clock cycle of the internal clock is completed (clock cycle measurement unit 1050), and setting an initial value of the delay amount of the variable delay addition circuit based on the duration time at the start of burst (column 23, lines 38-67).

Regarding claim 2: In so far as definite Matsuzaki teaches a semiconductor memory using a DDL circuit (FIG. 5) having a dummy delay (DUMMY-DATA-OUTPUT BUFFER

and DUMMY-INPUT BUFFER) corresponding to delay between an internal clock (the clock signal outputted from 1028) delay and an external clock (CLK), a variable delay addition circuit (the clock-cycle measurement unit without basic dleay1025, DELAY-CONTROL CIRCUIT 1040, 1022) having a means for adjusting delay amount by a delay amount adjusting signal (the signal outputted from DELAY-CONTROL CIRCUIT 1040), and a phase comparison circuit (PHASE COMPARISON CIRCUIT 1030) for comparing a phase of an internal clock (CLK2) with that of a delay clock (the internal clock outputted from 1028) inputted through the variable delay addition circuit and the dummy delay and outputting the delay amount adjusting signal (output from DELAY-CONTROL circuit 1040) to the variable delay addition circuit (input to 1022), the semiconductor memory comprising:

a means for inputting a first signal set to a logic “1” (START; FIG. 19, FIG. 20) outputted during one clock cycle of the internal clock to the variable delay addition circuit through the dummy delay at a start of burst (the DLL control circuit 1060 suspends the supply of CLK2 to the phase-comparison circuit, DLL, during a predetermined time period after a start of power supply to the semiconductor device or switching of operation mode from stand-by to a normal operation mode, burst mode is a normal operation mode such as read or write, and then the clock-cycle measurement unit 1050 measures a delay during one clock cycle of the clock CLK1 and outputs an obtained result to the delay-control circuit 1040; column 4, lines 5-12; column 23, lines 38-67; column 26, lines 1-19, and 64-67) ; and

a means for detecting duration time of the logic "1" of the first signal inputted from the variable delay addition circuit through the dummy delay addition circuit through the dummy delay until one clock cycle of the internal clock is completed (clock cycle measurement unit 1050; FIG. 19; FIG. 20), and setting an initial value of the delay amount of the variable delay addition circuit based on the duration time at the start of burst (column 23, lines 38-67).

Regarding claim 3: In so far as definite Matsuzaki teaches a semiconductor memory using a DDL circuit (FIG. 5) having a dummy delay (DUMMY-DATA-OUTPUT BUFFER and DUMMY-INPUT BUFFER) corresponding to delay between an internal clock (the clock signal outputted from 1028) delay and an external clock (CLK), a variable delay addition circuit (the clock-cycle measurement unit without basic delay1025, DELAY-CONTROL CIRCUIT 1040, 1022) having a means for adjusting delay amount by a delay amount adjusting signal (the signal outputted from DELAY-CONTROL CIRCUIT 1040), and a phase comparison circuit (PHASE COMPARISON CIRCUIT 1030) for comparing a phase of an internal clock (CLK2) with that of a delay clock (the internal clock outputted from 1028) inputted through the variable delay addition circuit and the dummy delay and outputting the delay amount adjusting signal (output from DELAY-CONTROL circuit 1040) to the variable delay addition circuit (input to 1022), the semiconductor memory comprising:

a means for inputting a first signal set to a logic "1" (START; FIG. 19, FIG. 20) during one clock cycle of the internal clock (CLK1) to the variable delay addition circuit through

the dummy delay at a start of burst (the DLL control circuit 1060 suspends the supply of CLK2 to the phase-comparison circuit, DLL, during a predetermined time period after a start of power supply to the semiconductor device or switching of operation mode from stand-by to a normal operation mode, burst mode is a normal operation mode such as a read or write, and then the clock-cycle measurement unit 1050 measures a delay during one clock cycle of the clock CLK1 and outputs an obtained result to the delay-control circuit 1040; column 4, lines 5-12; column 23, lines 38-67; column 26, lines 1-19, and 64-67) ; and

a means for detecting duration time of the logic "1" of the first signal inputted from the variable delay addition circuit through the dummy delay addition circuit through the dummy delay until one clock cycle of the internal clock (CLK1) is completed (clock cycle measurement unit 1050; FIG. 19; FIG. 20), and setting an initial value of the delay amount of the variable delay addition circuit based on the duration time at the start of burst (column 23, lines 38-67; start of a normal mode).

a clock outputting means for generating an output clock that synchronizes with the external clock one clock cycle behind with the internal clock delayed by the variable delay addition circuit and with the delay amount corrected by the phase comparison circuit as a lock mode after the initial setting of the delay amount in the variable delay addition circuit (column 18, lines 40-67 and column 19, lines 1-16).

Regarding claim 5: Matsuzaki teaches the semiconductor memory according to any one of claims 1 to 3 further comprising a means for setting externally the DLL circuit to

be used or not (FIG. 15; DLL CONTROL CIRCUIT in response to Spo or Spr suppresses the transmission of CLK2 to the DLL; hence, not using the DLL; column 23, lines 29-67; column 24, lines 1-15).

Regarding claim 6: In so far as definite Matsuzaki teaches a semiconductor memory using a DDL circuit (FIG. 5) having a dummy delay (DUMMY-DATA-OUTPUT BUFFER and DUMMY-INPUT BUFFER) corresponding to delay between an internal clock (the clock signal outputted from 1028) delay and an external clock (CLK), a variable delay addition circuit (the clock-cycle measurement unit without basic delay1025, DELAY-CONTROL CIRCUIT 1040, 1022) with a means for adjusting delay amount by a delay amount adjusting signal (the signal outputted from DELAY-CONTROL CIRCUIT 1040), and a phase comparison circuit (PHASE COMPARISON CIRCUIT 1030) for comparing a phase of an internal clock (CLK2) with that of a delay clock (the internal clock outputted from 1028) inputted through the variable delay addition circuit and the dummy delay and outputting the delay amount adjusting signal (output from DELAY-CONTROL circuit 1040) to the variable delay addition circuit (input to 1022), the semiconductor memory comprising:

a means for inputting a first signal set to a logic "1" (START; FIG. 19, FIG. 20) during one clock cycle of the internal clock (CLK1) to the variable delay addition circuit through the dummy delay at a start of burst (the DLL control circuit 1060 suspends the supply of CLK2 to the phase-comparison circuit, DLL, during a predetermined time period after a start of power supply to the semiconductor device or switching of operation mode from

stand-by to a normal operation mode, burst mode is a normal operation mode such as read or write, and then the clock-cycle measurement unit 1050 measures a delay during one clock cycle of the clock CLK1 and outputs an obtained result to the delay-control circuit 1040; column 4, lines 5-12; column 23, lines 38-67; column 26, lines 1-19, and 64-67) ; and

a means for detecting duration time of the logic "1" of the first signal inputted from the variable delay addition circuit through the dummy delay addition circuit through the dummy delay until one clock cycle of the internal clock (CLK1) is completed (clock cycle measurement unit 1050; FIG. 19; FIG. 20), and setting an initial value of the delay amount of the variable delay addition circuit based on the duration time at the start of burst (column 23, lines 38-67; start of a normal mode);

a clock outputting means for generating an output clock that synchronizes with the external clock one clock cycle behind with the internal clock delayed by the variable delay addition circuit and with the delay amount corrected by the phase comparison circuit as a lock mode after the initial setting of the delay amount in the variable delay addition circuit (column 18, lines 40-67 and column 19, lines 1-16); and

a means to switch the DLL circuit between use and nonuse by user setting with a command decoder (FIG. 13; 1102, 1103,1104) for decoding an address signal for specifying a user-specified command and a data signal for specifying a user-specified command (a READ or a WRITE or a power-on), and a command register (MODE REGISTER) for storing the output of the command decoder as the lock mode after the

initial setting of the delay amount in the variable delay addition circuit (FIG. 13; column 20, lines 6-32; column 23, lines 29-67; column 24, lines 1-15).

Regarding claim 8: Matsuzaki teaches the semiconductor memory according to any one of claims 1, 2, 3 or 6 further comprising a reset means for resetting the DLL circuit at the start of burst (interpreted to mean a read or write operation; for example when returning from standby to start a normal operation such as a read or write the DLL circuit is reset in the sense that the clock cycle-measurement unit measures a delay in one clock cycle of the external clock signal and outputs a result to the delay-control circuit which then performs an initial setting of the variable delay circuit. Thereafter, operations of the DLL circuit are in normal a operation such as read or write operation; column 23, lines 29-67; column 24, lines 1-15).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuzaki in view of Yamazaki (US 6,198,689 B1; hereinafter "Yamazaki").

Regarding claim 4: Matsuzaki teaches the semiconductor memory according to any one of claims 1 to 3, wherein the DLL circuit can implement a standby mode when a reading operation is not performed, and output readout data in an extremely short time from the start of the reading operation (column 2, lines 52-62; column 16, lines 60-67; column 17, lines 1-6; column 18, lines 40-65).

Matsuzaki teaches the frequency of the clocks including the external clock are lower in the standby mode but does not specifically teach the external clock and the internal clock are completely stopped when a reading operation is not performed.

Yamazaki teaches (FIG. 6) in a standby mode, which is a power down operation, the external clock and the operation of the DLL circuit are stopped to save power (column 6, lines 49-61).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the teaching of Yamazaki into the memory of Matsuzaki in a manner such that the external clock and the internal clock would be completely stopped when a reading operation is not performed such as in standby. The motivation to do so would have been to save more power by stopping completely the operation of the external clock and the DLL while in the standby mode.

Allowable Subject Matter

11. Claim 7 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 7: The prior art made of record and considered pertinent to the applicant's disclosure, taken individually or in combination, does not teach or suggest the claimed limitation of the semiconductor memory further comprising a means for automatically setting a latency one clock shorter than the clock latency set by the user and making the latency when seen externally the same as that set by the user in combination with the other limitations thereof as is recited in the claim.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAY RADKE whose telephone number is (571)270-1622. The examiner can normally be reached on Monday-Friday 7:30AM-5:00PM EST, Alternate Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571)272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. R./
Examiner, Art Unit 2827
/AMIR ZARABIAN/
Supervisory Patent Examiner, Art Unit 2827